REMARKS:

Applicant has carefully studied the nonfinal Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicant responds to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Drawing Objections

The Office has objected to the drawings under 37 CFR 1.83(a). The Office states that the steps of creating a PN-junction throughout the surface of the wafer and then forming recessed areas characterized by the absence of the surface PN-junction are not clearly shown in the drawings. The Office concludes that these features must be clearly shown in the drawings or canceled from the claims. The Office admits that while the claim limitations are shown, the drawings are hard to read and therefore it is unclear where the p-type and n-type regions are, and where the presence/absence of the surface PN-junction is.

Accordingly, corrected drawings sheets in compliance with 37 CFR 1.121 (d) have been submitted with this response to the Office Action to avoid abandonment of the application.

Fig. 1 has been amended to more clearly identify the PN-junction 15 that is created through out the surface of the wafer by diffusing a P-type dopant into an N-type silicon wafer 10. Diffusion to create a PN-junction is well known in the art and is described within the specification as filed. Accordingly, no new matter has been added.

Fig. 2 has been amended to more clearly identify the thin layer of oxide **20** that is sputtered and patterned using the desired mask on top of the diffusion in relation to the surface PN-junction **15**. No new matter has been added.

Fig. 3 has been amended to more clearly identify the step of subjecting the substrate to KOH etching for ten minutes to create recessed areas **25** where the oxide was patterned in relation to the PN-junction **15**. Element **30** was removed from this figure, because the porous silicon **30** is has not yet been formed. The patterning of oxide and the silicon beneath creates patterns of the surface, which are contrasted by the presence and absence of PN-junction. No new matter has been added.

Fig. 4 has been amended to clearly identify the formation of the porous silicon **30** in relation to the PN-junction **15**. As shown in amended Fig. 4, and detailed in the specification as filed, porous silicon **30** is formed on the patterned wafer using HF based electrochemical etching technique. The pores are formed in areas that are characterized by the absence of surface junction. In the areas which have a surface junction, the junction blocks the pore initiation and propagation due to lack of holes in the depletion region, which are essential to porous silicon formation. The resultant wafer is selectively porous in the areas where the oxide was patterned and the rest of the wafer is bulk silicon. No new matter has been added.

Fig. 5 has been amended to more clearly identify the step of KOH or TMAH etching the wafer for thirty seconds which results in rapid dissolution of porous areas **30**, leaving behind bulk silicon, thus resulting in through wafer high aspect ratio structures with straight sidewalls **35**. No new matter has been added.

Claim Rejections – 35 U.S.C. § 112

The Office has rejected claims 1, and 4-14 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Office states that it is unclear how there can be an absence of a PN junction since the claims defines that a PN-junction is created throughout the surface of the wafer. And as such, the metes and bounds of the claims are unclear. The Office further questions the terminology, "absence of a PN-junction", and asks whether both p-type and n-type regions need to be removed, or only either the p-type or the n-type region?

In response, claim 1 has been amended to positively recite the method steps of the invention in a specific order and to further clarify the etching step as being sufficient to etch away the surface PN-junction created by the prior diffusion step, thereby creating recessed areas characterized by the absence of a surface PN-junction.

Additionally, as described in an exemplary embodiment of the specification as filed, an N-type silicon wafer **10** is diffused with P-type dopant to the order of 1020 atoms/cm^2 to create a blanket PN-junction **15** throughout the surface of the wafer. After the surface is patterned with the oxide layer, the wafer is then subjected to KOH etching for ten minutes to create recessed areas **25** where the oxide was patterned. The patterning of oxide and the silicon beneath creates patterns on the surface, which are contrasted by the presence and absence of PN-junction. It is clear from this exemplary embodiment that the step of etching to create recessed areas is dependent upon the diffusion step previously performed to create the PN-junction. It is well known in the art that varying the diffusion temperature and duration will result in varying depths of the PN-junction into the surface of the wafer. Based on the specifics of the diffusion, the duration of the etching step is varied to allow sufficient time for removal of the PN-junction.

As such, Applicant believes that the amended claims would enable one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, to ascertain the claims with a reasonable degree of precision and particularity. Accordingly, Applicant believes that claims 1, and 4-14 are definite under 35 U.S.C. § 112, second paragraph, and that the claims particularly point out and distinctly claim the subject matter which applicant regards as the invention and are now believed to be in condition for allowance.

Claim Rejections – 35 U.S.C. § 102

Applicant acknowledges the quotation of 35 U.S.C § 102(b).

Claims 1, 4-7, 9 and 11-12 stand rejected under 35 U.S.C § 102(b) as being clearly anticipated by Ishida et al. (U.S. Patent No. 5,830,777). Applicant respectfully submits that Ishida et al. does anticipate as the reference does not contain all the elements recited in the claims at bar.

With specific reference to Claim 1, the Office states that Ishida discloses a method comprising the steps providing a silicon wafer **2**; diffusing the wafer with dopant (to form p+ region **3**, Fig. 5), whereby the diffusion creates a PN-junction throughout the surface of the wafer (forming n-type layer **5**, Fig. 6); providing a mask **20a** (Fig. 5); positioning the mask **20a** in overlying relation to the surface of the wafer; patterning a layer of oxide **22** on the surface of the wafer (with openings **22a**, Fig. 7); etching the wafer to create recessed areas **4** coincident with the patterned oxide (Fig. 10), the recessed areas characterized by the absence of surface PN-junction (regions where openings **22a** are before the doping step of Fig. 7); hydrofluoric acid etching the wafer to form porous silicon **24** thereon, whereby the porous silicon is formed coincident with the surface area characterized by the absence of surface PN-junction (since the porous silicon is defined in part by the region **23**); subjecting the wafer surface to wet etching resulting in dissolution of the porous silicon (Fig. 10).

Applicant respectfully submits that Ishida et al. does not anticipate amended claim 1 because Ishida et al. does not describe the steps of the present invention in the order as claimed, and Ishida does not describe the steps of etching the wafer to create recessed areas coincident with the patterned oxide, whereby the etching step is sufficient to etch away the surface PN-junction created by the diffusion step, thereby creating recessed areas characterized by the absence of surface PN-junction, and hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the porous silicon is formed coincident with the surface wafer area characterized by the absence of surface PN-junction.

More specifically, Ishida et al. does not describe a diffusion step to create a surface PN-junction, followed by an etching step to etch away the created surface PN-junction in selected areas of the substrate as identified by a mask thereby creating recessed areas characterized by the absence of surface PN-junction, and hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the porous silicon is formed coincident with the surface wafer area characterized by the absence of surface PN-junction.

As such, Applicant respectfully submits that Ishida et al. does not anticipate the present invention because it does not describe the steps of etching the wafer to create recessed areas coincident with the patterned oxide, the recessed areas characterized by the absence of a surface PN-junction, and hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the

porous silicon is formed coincident with the surface area characterized by the absence of the surface PN-junction.

For the reasons cited above, Applicant believes that amended independent claim 1 is not anticipated by Ishida and is believed to be in condition for allowance.

Claims 4-14 are dependent upon claim 1, and are therefore allowable as a matter of law.

Claim 15 has been added in this amendment to further define a method step of claim 1. As such, claim 15 is dependent upon claim 1, and is therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned at (813) 925-8505 is requested.

Very respectfully,

SMITH & HOPEN

By:_____

Dated: August 21, 2006

Molly L. Sauter
USPTO Reg. No. 46,457
180 Pine Avenue North
Oldsmar, Florida 34677
(813) 925-8505
Agent for Applicants

RECEIVED
CENTRAL FAX CENTER
AUG 21 2006

CERTIFICATE OF FACSIMILE TRANSMISSION
(37 C.F.R. 1.8(a))

I HEREBY CERTIFY that this Amendment B, including Amendments to the Claims, and Remarks is being transmitted by facsimile to the United States Patent and Trademark Office, Art Unit 1765, Attn.: Anita Karen Alanko, (571) 273-8300 on August 21, 2006.

Dated: August 21, 2006

April Turley
April Turley